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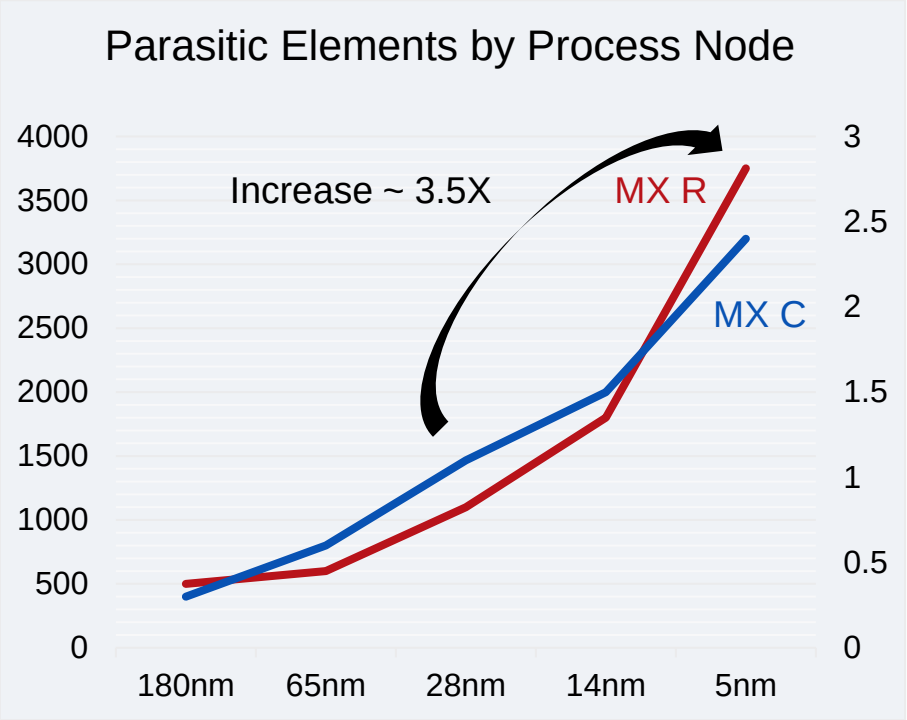
Jivaro Pro

Parasitic Reduction to Accelerate SPICE simulations

Jivaro Pro

Introduction

- As process geometries grow smaller the number of parasitic elements grow at a dramatic rate
- While these parasitic elements must be accounted for, they can have a significant negative impact on the simulation time of a given circuit
- Design tools with built-in parasitic reduction can help reduce simulation times but these solutions deliver far less performance, modularity and productivity improvement than Jivaro Pro
- Jivaro Pro is a best-in-class stand-alone parasitic reduction solution that can reduce simulation times from days to hours !!

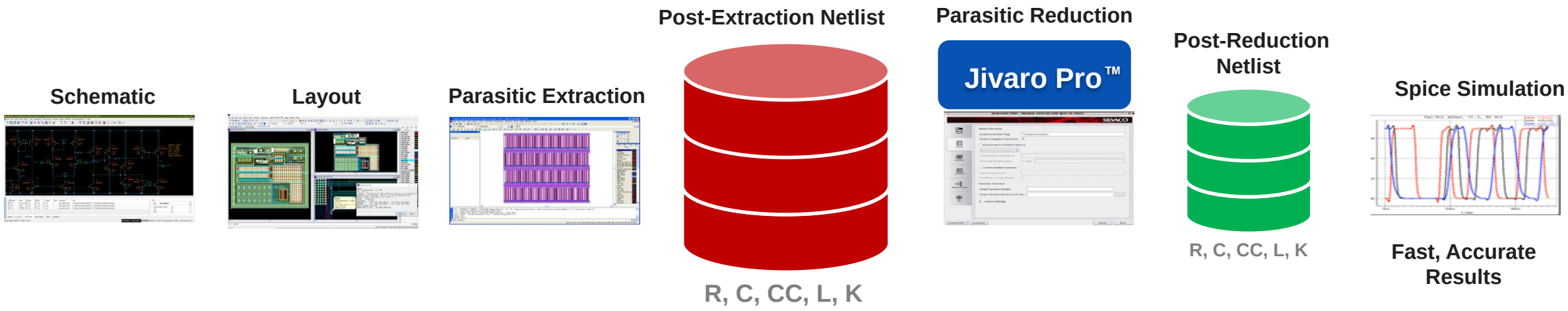


Aggregation of publicly available data

Jivaro Pro Netlist Parasitic Reduction

Overview and Benefits

- Up to 2-15X faster SPICE simulation with the same accuracy
  - Significantly reduce post-extraction netlists
  - Accelerate your design cycle and increase productivity
  - Increase coverage via more simulations (run several per day instead of one)
  - Minimize compute resources and development costs (i.e., CPU and Memory configuration)



Jivaro Pro Works for All Design Types and Process Nodes

Design Flexibility

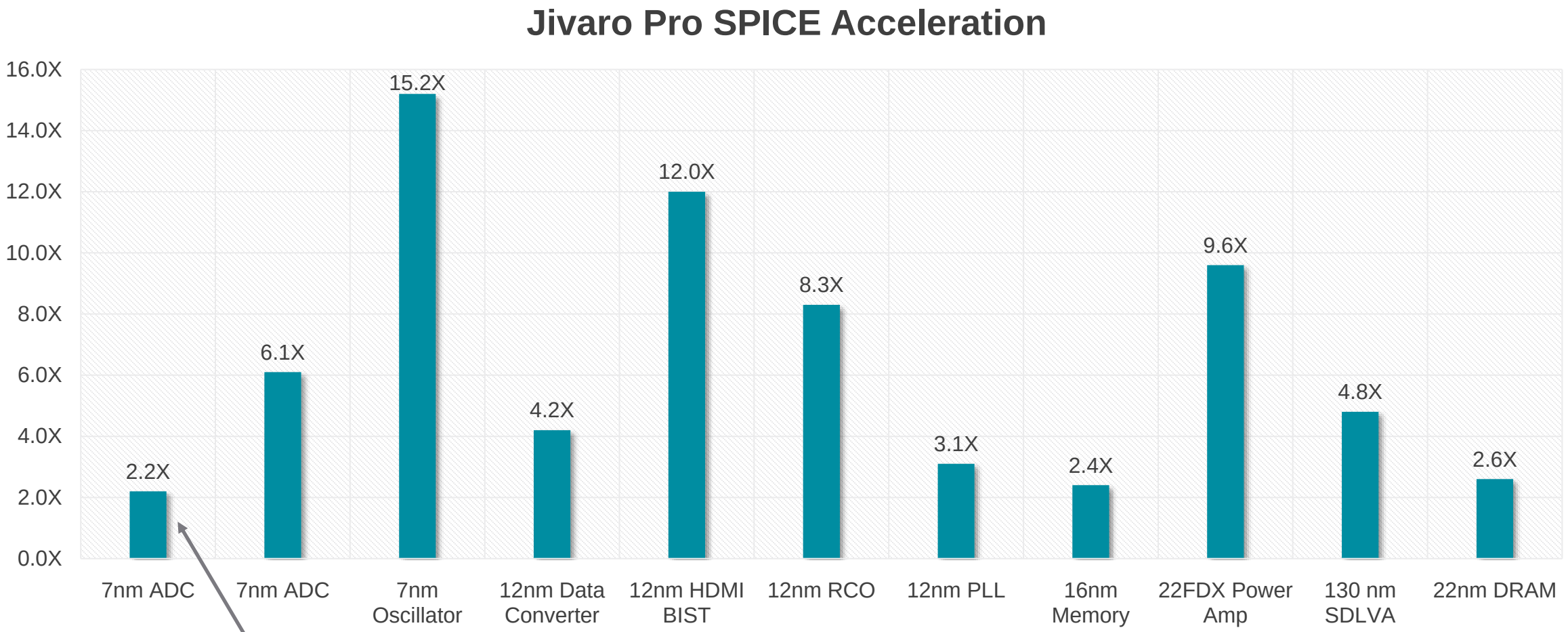
- Process / technology node agnostic
  - Only works on the parasitic netlist or DB
  - Any geometry
  - Planar or FinFET
  - Silicon proven

65nm	40nm	28nm	20nm	14nm	10nm	7nm	5nm	3nm
✓	✓	✓	✓	✓	✓	✓	✓	✓

- Design examples:
  - ADC (Analog to Digital Converter)
  - AFE (Analog Front End)
  - DAC (Digital to Analog Converter)
  - PLL (Phase Locked Loop)
  - DLL (Delay Locked Loop)
  - VCO (Voltage-Controlled Oscillator)
  - CTLE (Continuous Time Linear Equalizer)
  - LDO (Low Dropout)

Jivaro Pro Delivers Superior SPICE Acceleration

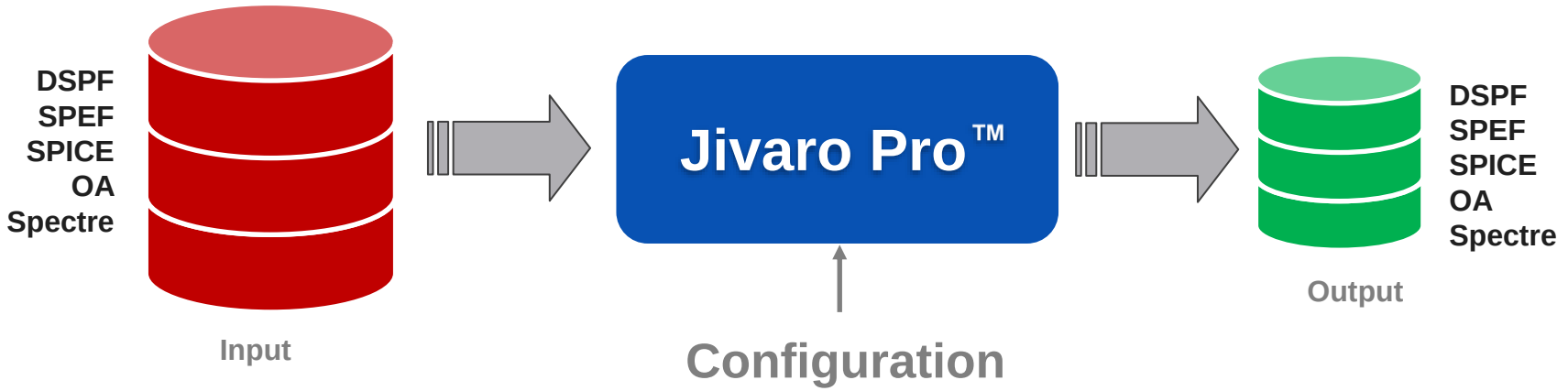
SPICE Acceleration



20 minutes of Jivaro Pro runtime saved 7 days of simulation runtime
(14-day runtime reduced to less than 7 days)

Netlist-to-Netlist Parasitic Reduction

Enables Seamless Workflow Integration



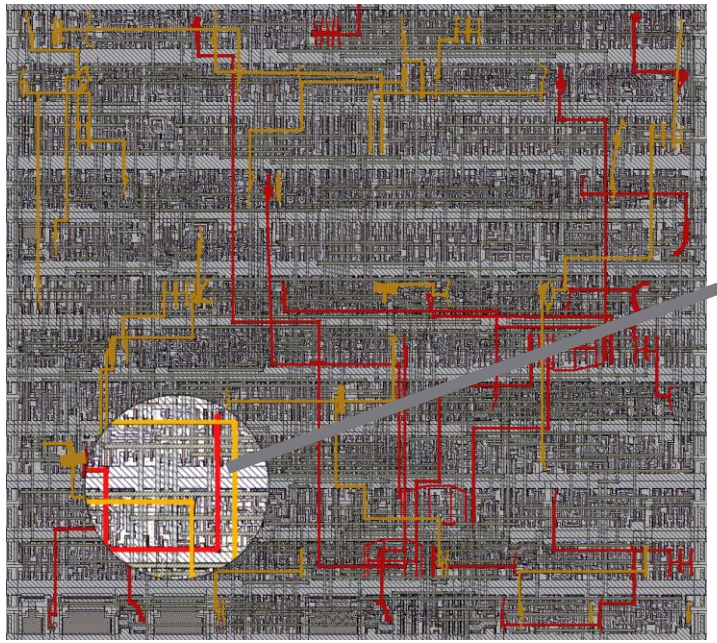
- All major input formats supported
  - DSPF, SPEF, Spice, Spectre and Open Access
  - Netlist in -> netlist out solution
- Configurable reduction rate and accuracy
  - Specify overall reduction/accuracy criteria
  - Selectively apply criteria within the design

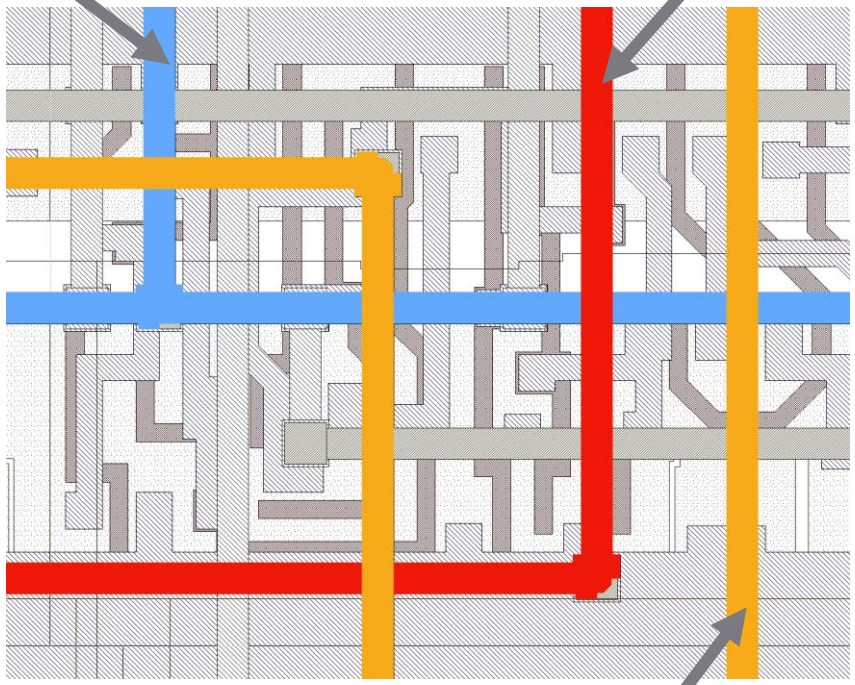
- Auto mode for easy access to advanced features:
  - Powerful and accurate reduction of floating nets
  - Auto-tuned decoupling of coupling capacitances
  - Automatic power net detection w/selective reduction
  - Intelligent and accuracy-controlled multi-finger device merging
  - FinFET dummy device removal

Target Your Parasitic Reduction

Specify Where and How to Apply Reduction Criteria

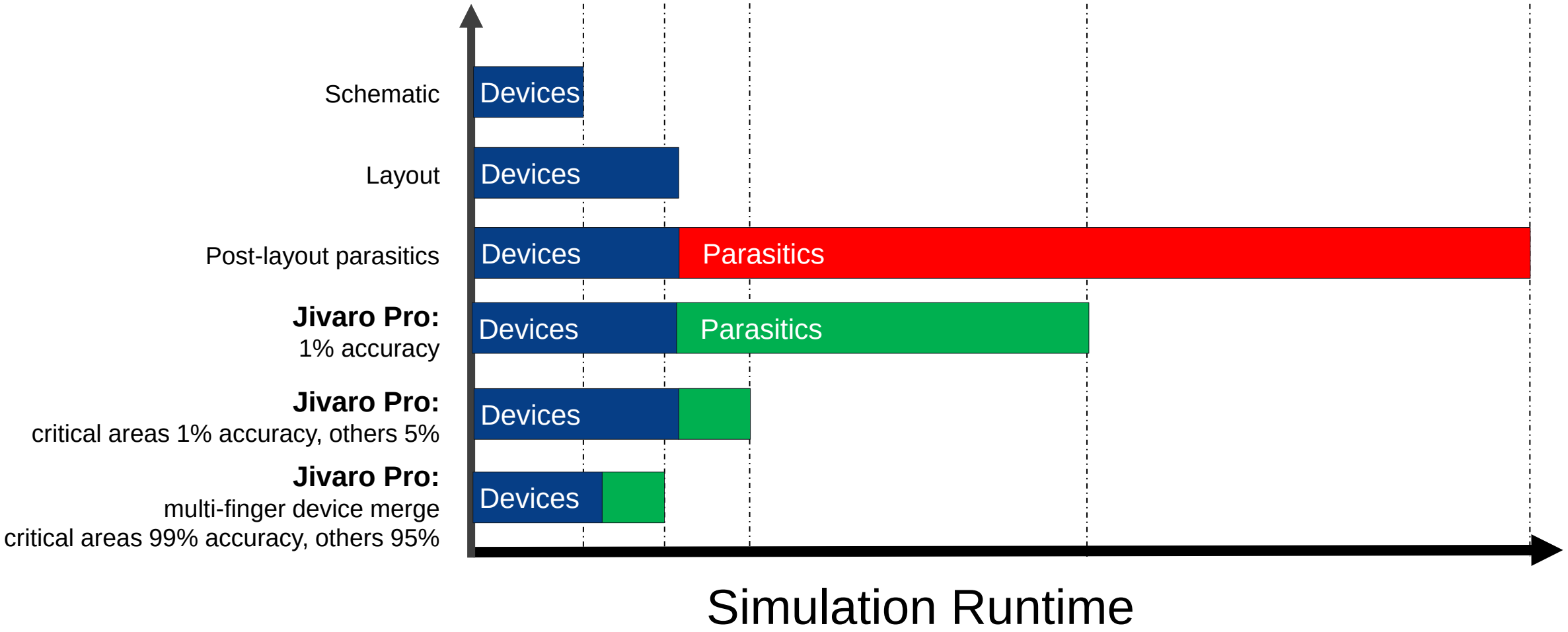
- User customizable, selective reduction
  - Apply different settings to different parts of the design
  - By nets, paths or hierarchically by subcircuit
  - Accuracy parameters are fully customizable for all nets





Jivaro Pro Parasitic Reduction

Multi-finger device and dummy device merge and removal



Jivaro Pro, Real-World Application

Analog block, 10k transistors, 5nm

- **Application of Jivaro Pro in a Top 10 company post-extraction flow**
  - Customer engaged in an evaluation and realized a **4X improvement in runtime while meeting accuracy requirements.** This led to a permanent deployment of Jivaro Pro in their flow
- Installation of Jivaro Pro into their flow took less than one day

Reduction Strategy		Transient Simulation Time	PD Gain	Static Phase Offset	Power	Output Ripple
No reduction	-	5.11hrs	45.75GV/s	5.66ps	7.33mA	3.73mV
PEX reduction	reduction = YES pwr reduction = HIGH	4.98hrs	45.76GV/s	5.88ps	7.34mA	3.77mV
Jivaro Pro	errorMax 0.5 frequencyLimit 90 criterion auto	**2.64hrs**	**45.72GV/s**	**5.64ps**	**7.26mA**	**3.55mV**
	errorMax 2 frequencyLimit 90 criterion auto	**1.23hrs**	**45.4GV/s**	**5.49ps**	**7.30mA**	**3.48mV**

Jivaro Pro, Real-World Application

Analog Block, 2M Transistors, 5nm

- **A second example of the simulation runtime benefits with Jivaro Pro**
  - With embedded reduction in extraction. (not recommended, but still effective)
  - 20+ day simulation reduced to 10 days while maintaining accuracy

Reduction Strategy		Transient Sim Time	Initial VCO amplitude	Initial VCO frequency	HS_RVDD current	LS_RVDD current
PEX reduction	reduction = HIGH pwr reduction = HIGH	500hrs	827.8mV	25.69GHz	14.33mA	3.51mA
PEX reduction + **Jivaro Pro**	reduction = HIGH pwr reduction = HIGH errorMax 0.5 frequencyLimit 60 criterion auto	**240hrs**	**832.7mV**	**25.64GHz**	**14.37mA**	**3.49mA**

Jivaro Pro Summary

Summary

- Today's flows with built-in parasitic reduction in extraction and simulation do little to improve simulation speeds or increase design productivity

- Jivaro Pro enables 2-15X post-layout SPICE simulation speedups while maintaining accuracy
  - Easy plug-n-play into existing flows
  - Enables running the largest or previously impossible simulations
  - Include power nets and metal fills in simulations for greater accuracy
  - Customize the parasitic reduction to meet *your* objectives
  - Increase coverage via more simulations. Make your designer more productive
  - Minimize compute resources (i.e., CPU and Memory configuration)

- Accelerate your design cycle and increase productivity with Jivaro Pro


Thank you
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